

FIG. 1

1/12

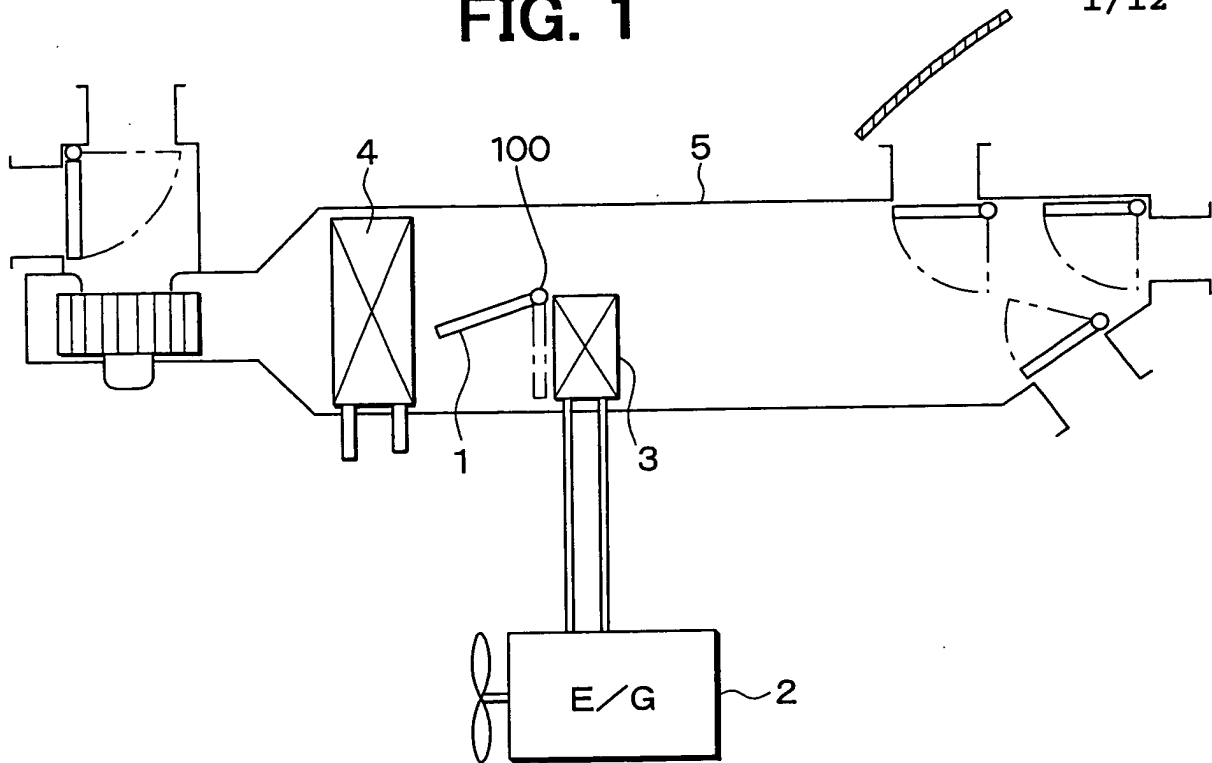


FIG. 2

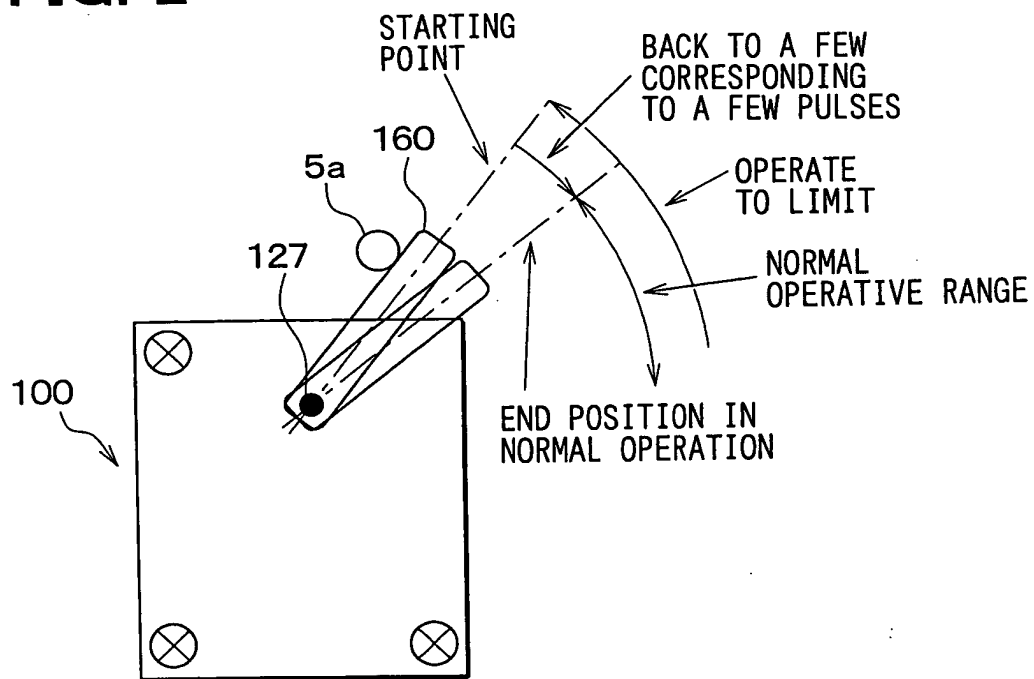


FIG. 3

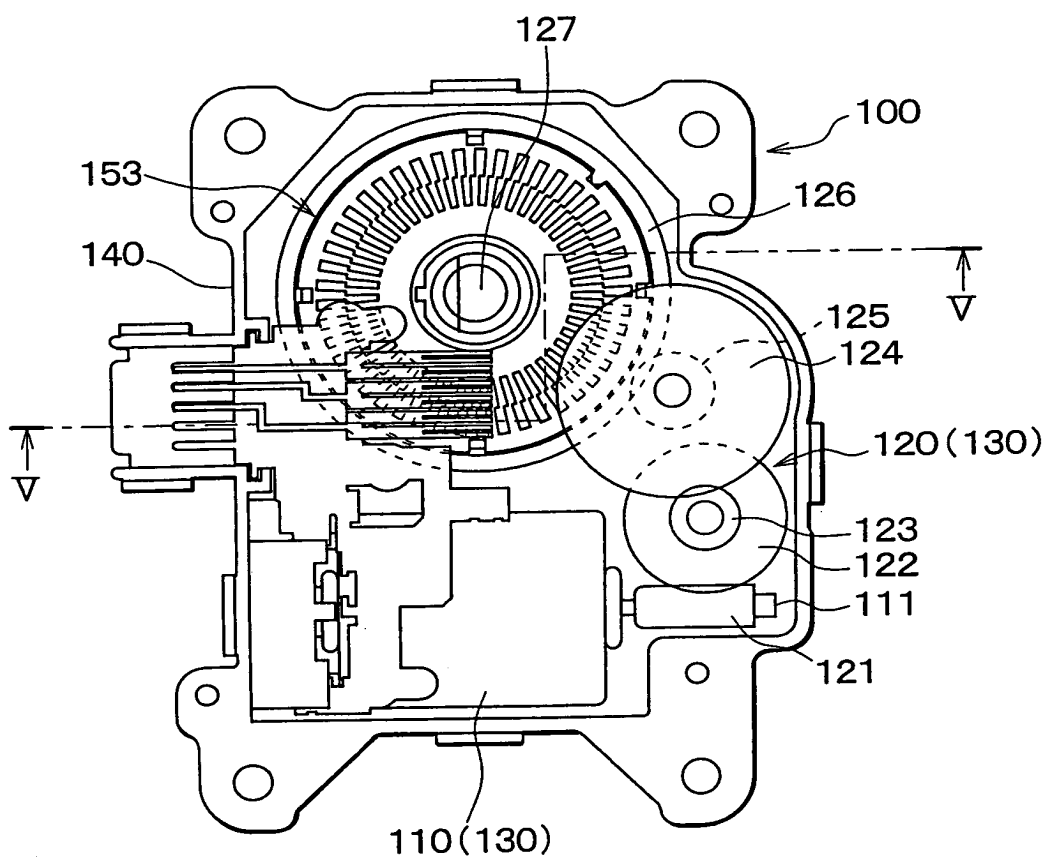


FIG. 4A

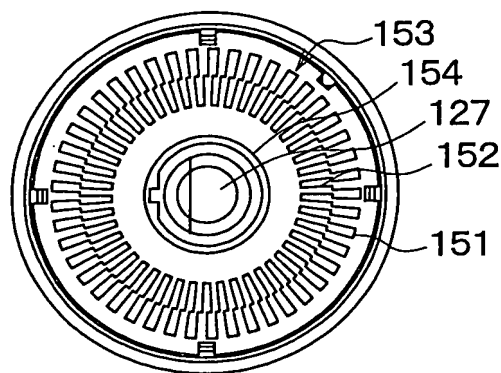


FIG. 4B

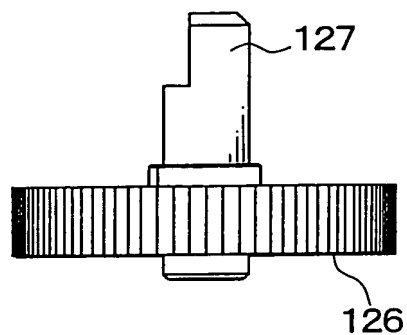


FIG. 5

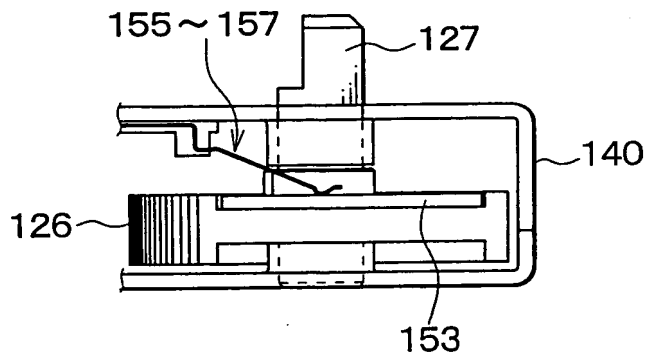


FIG. 7 is a block diagram of a motor control system. The system includes a CPU, a MOTOR CNTL. (Motor Control), a MEMORY, a PULSE COUNT, and a PULSE DETECTOR, all connected to a BATTERY and a COMMON ground. The CPU is connected to a CONSTANT VOLT. source. The MOTOR CNTL. is connected to the MOTOR DRIVER. The MEMORY is connected to the PULSE DETECTOR. The PULSE COUNT is connected to the PULSE DETECTOR. The PULSE DETECTOR is connected to the COMMON ground. The MOTOR DRIVER is connected to the MOTOR (110). The MOTOR is connected to the COMMON ground. The PULSE DETECTOR is connected to the COMMON ground. The PULSE COUNT is connected to the PULSE DETECTOR. The MEMORY is connected to the PULSE DETECTOR. The MOTOR CNTL. is connected to the MOTOR DRIVER. The CPU is connected to the CONSTANT VOLT. source. The BATTERY is connected to the CPU and the MOTOR DRIVER. The COMMON ground is connected to the MOTOR and the PULSE DETECTOR.

FIG. 8

$\alpha/2$ α β ($\alpha = \beta$)

PULSE PATTERN
FORWARD DIRECTION

PRINT
SUBSTRATE

PATTERN
(CONDUCTIVE
PORTION)

A-PHASE: +
COMMON: GND
B-PHASE: +

SIGNAL PATTERN No.

| No. | 1a | 2a | 3a | 4a | 1b | 2b | 3b | 4b |
|--------|----|----|----|----|----|----|----|----|
| A-PHA. | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| B-PHA. | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

FIG. 9

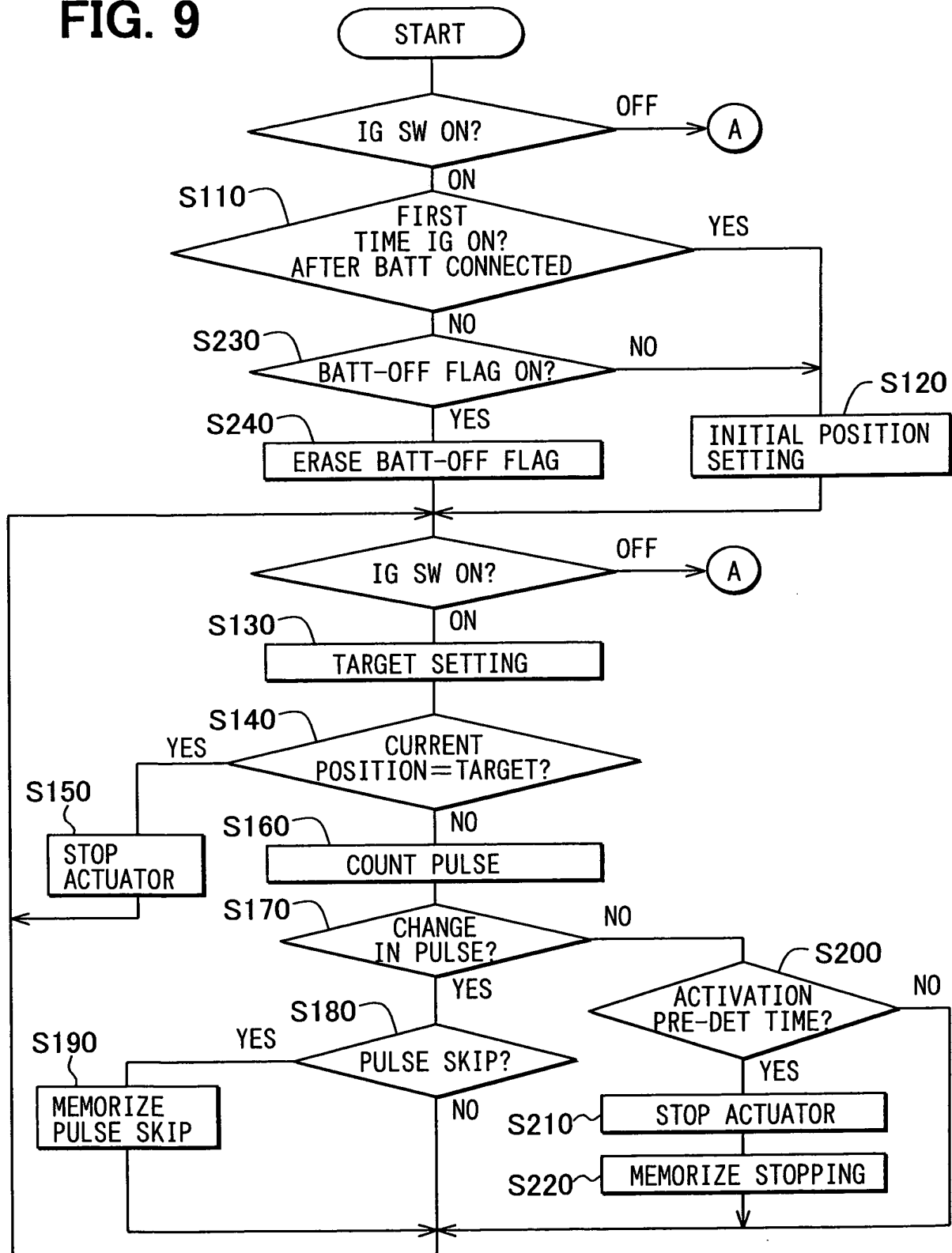


FIG. 10

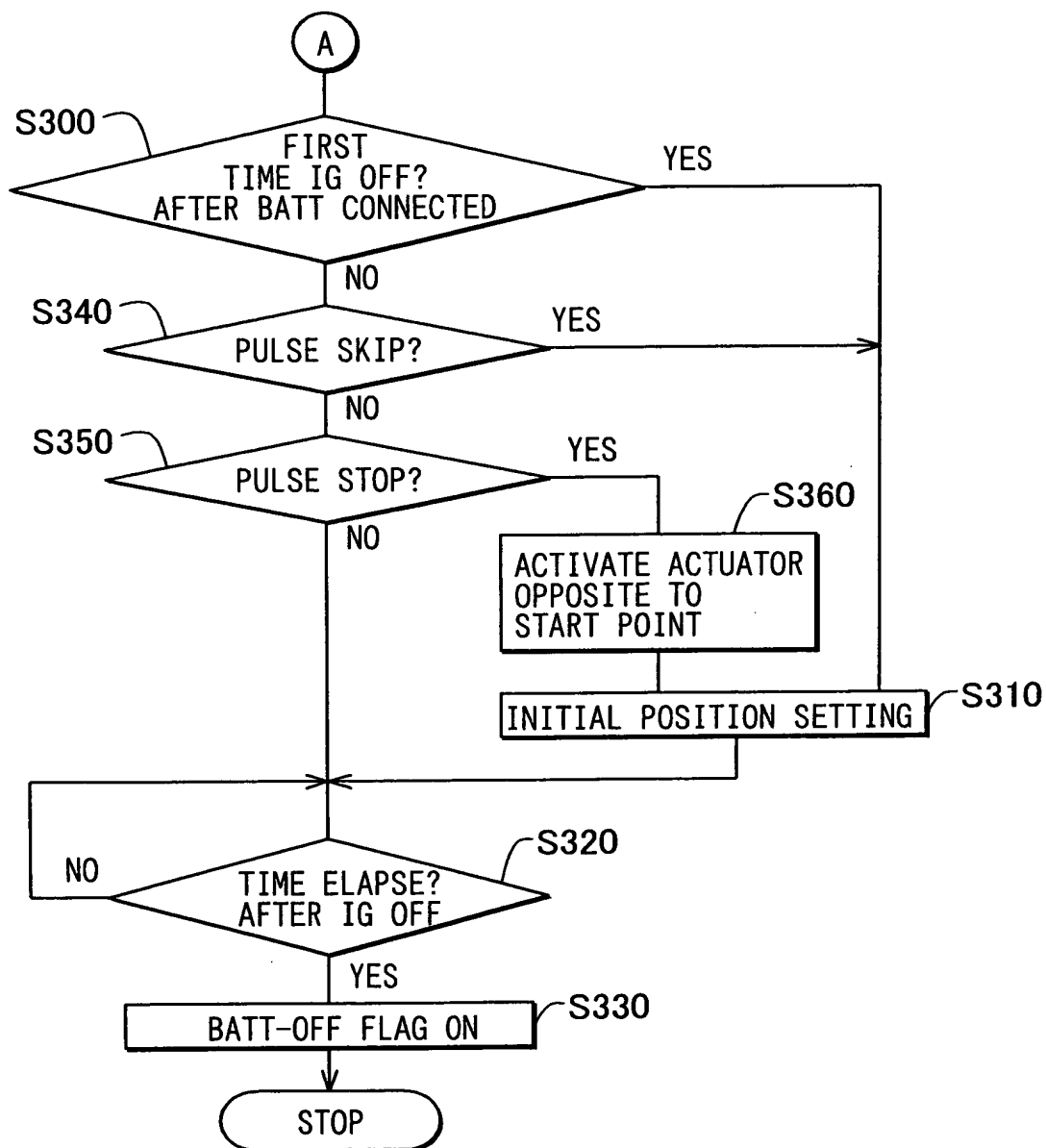


FIG. 11

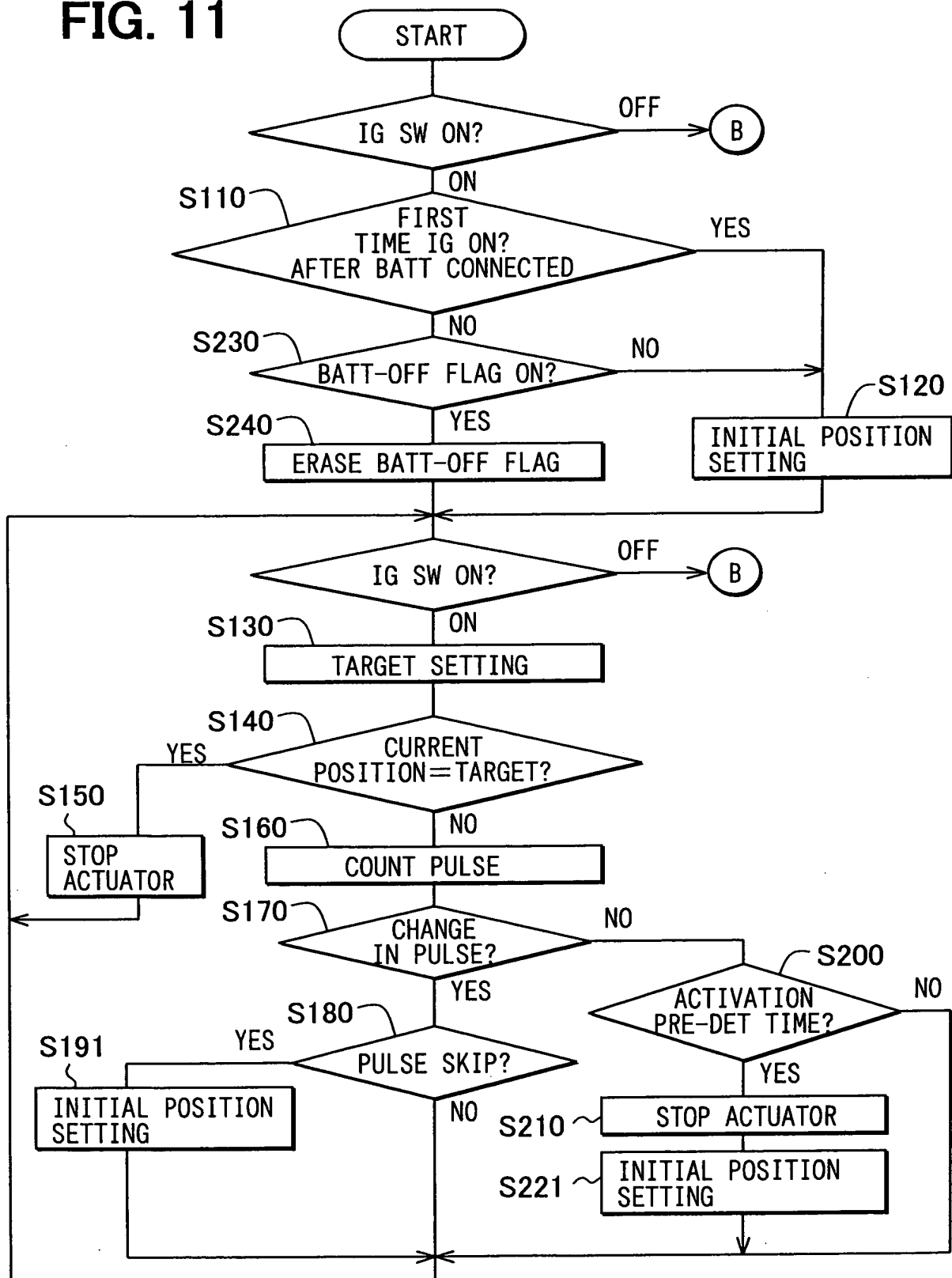


FIG. 12

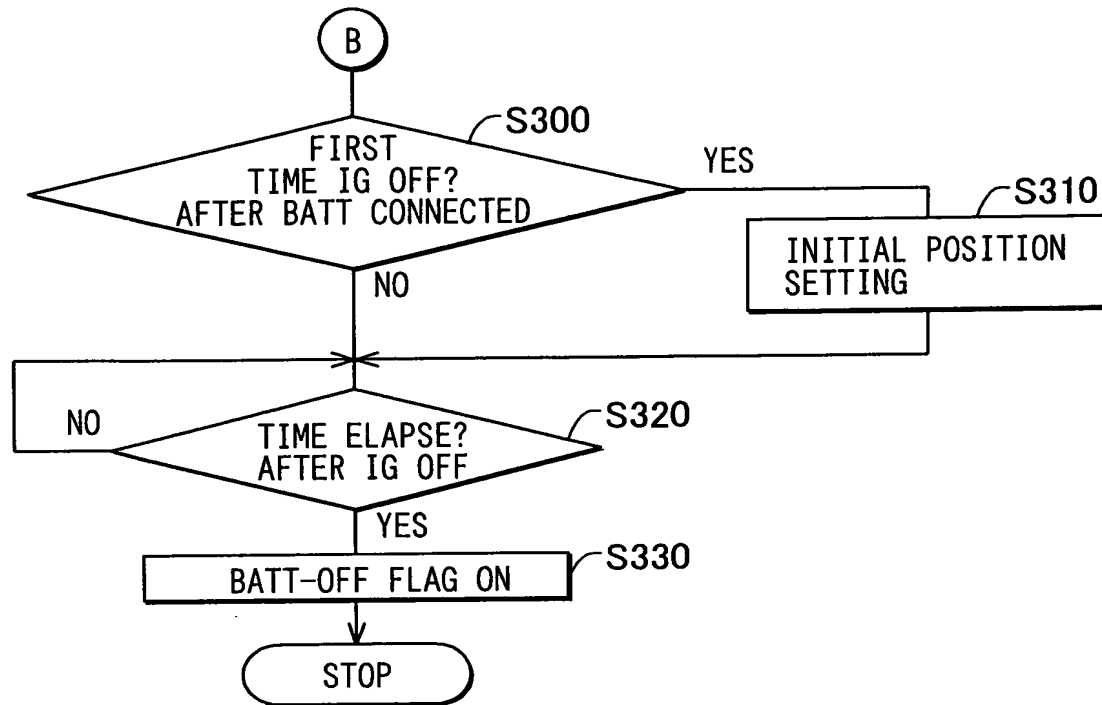


FIG. 13

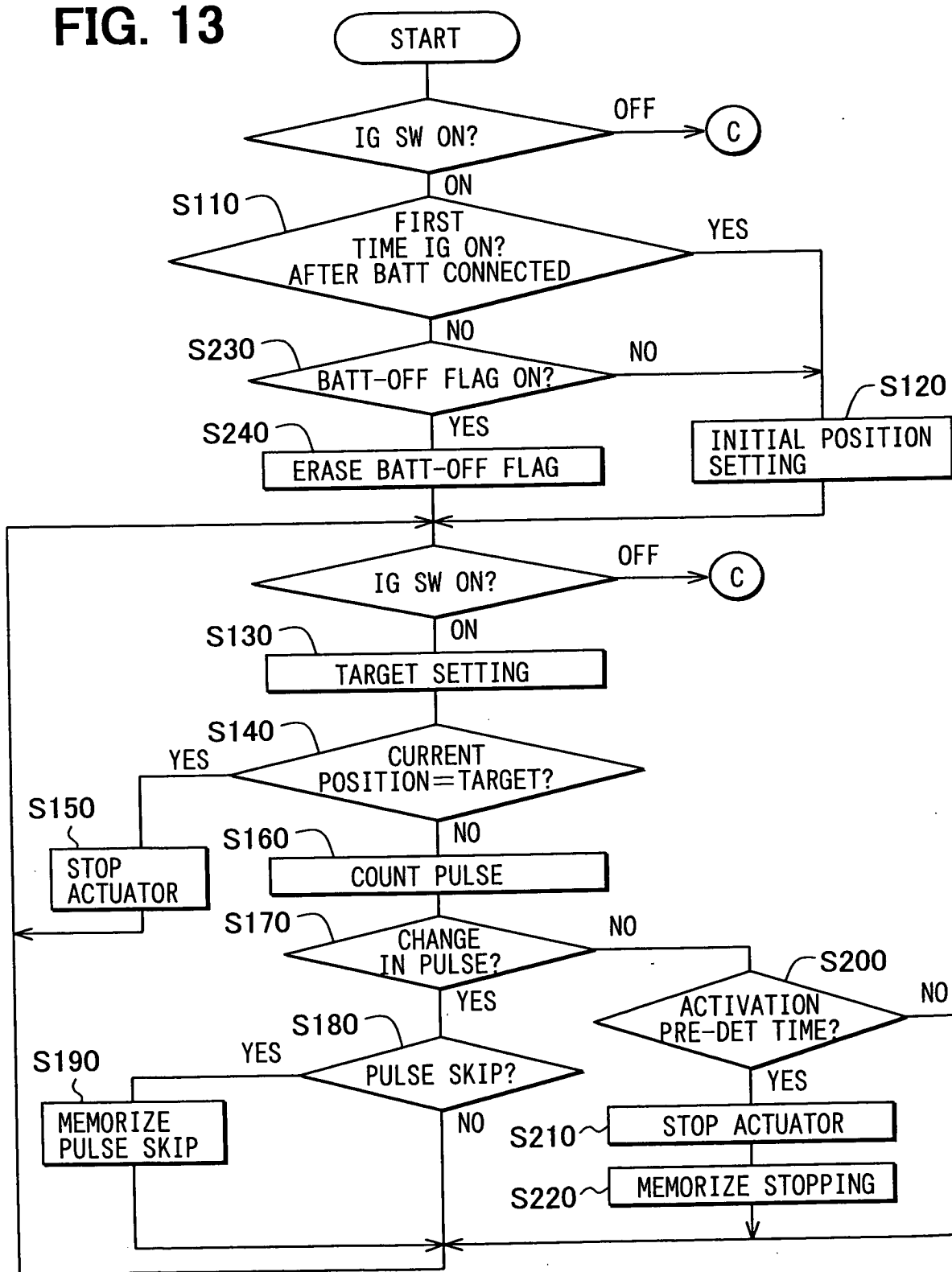


FIG. 14

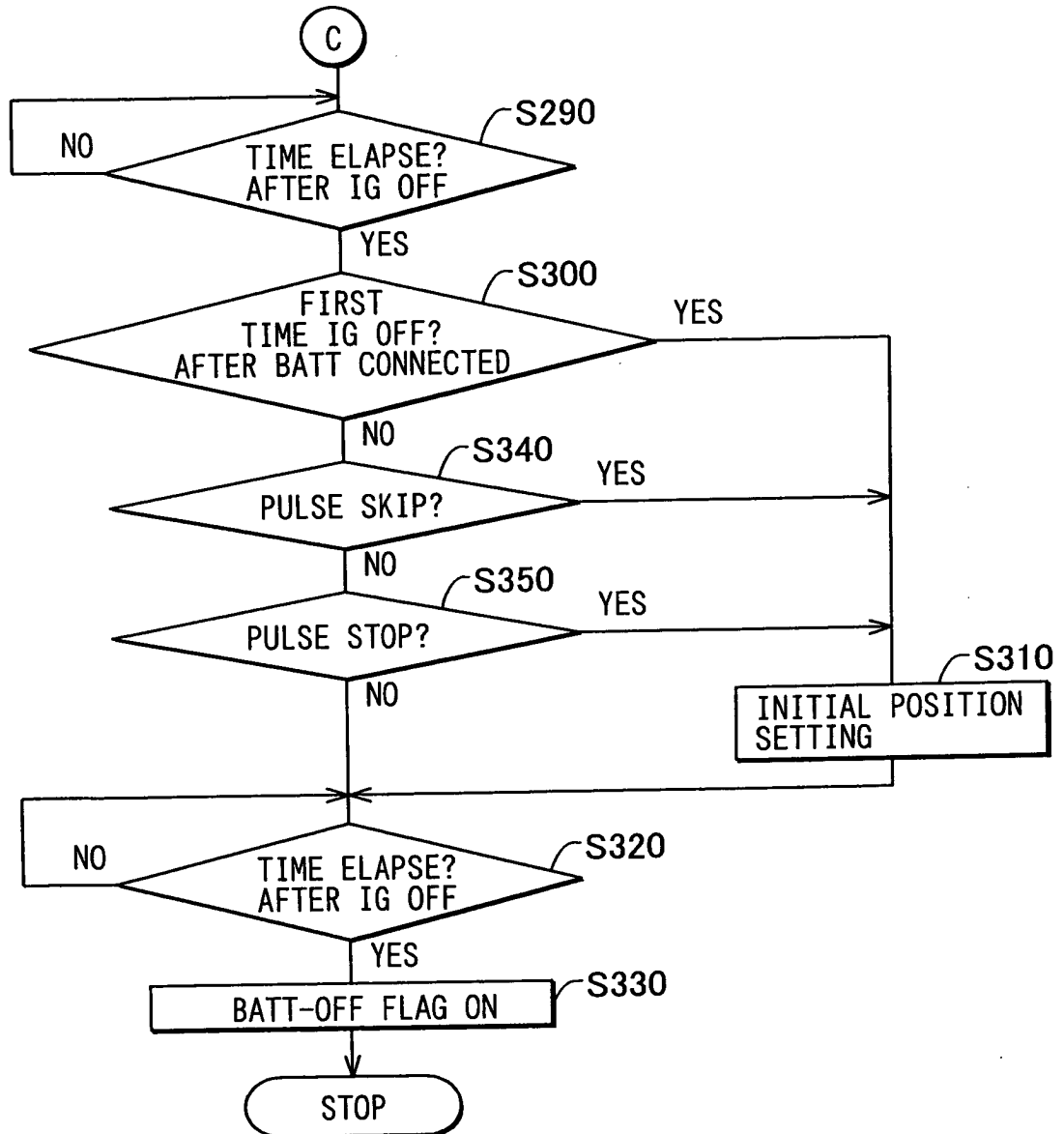


FIG. 15

